David Zambrano

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EDUCATION

Florida Polytechnic University, Lakeland, FL

Bachelor of Science in Computer Engineering – *GPA: 3.88* May 2026

Master of Science in Electrical Engineering – *GPA: 3.5* Graduating May 2027

PROFESSIONAL EXPERIENCE

Undergraduate Research Assistant | *Bin Tarik Nanophotonics Group* May 2025 – Present

- Designed a novel optical ring resonator for enhanced coupling performance & all-optical logic gates (NOT, NAND, NOR), operating at the center of the optical C-band range (1550nm).
- Utilized Flexcompute's Tidy3D Python library for device geometry specification and electromagnetic simulation, and KLayout for GDSII layout editing for fabrication on 220nm Silicon-on-Insulator (SOI) process.

R&D Intern | *Measutronics Corporation* May 2024 – Aug 2024

- Created an alarm system for dredging vehicles using programmable logic controller (PLC) technology, to warn of hazardous/restricted zones not immediately visible by dredging vehicle operators.
- Utilized microcontroller programming skills to create a robust system, complete with GUI for user configuration.

DESIGN PROJECTS

Cascadable All-Optical Logic Gates | *Bin Tarik Nanophotonics Group* May 2025 – Present

- Designed an all-optical inverter from microring resonators, utilizing destructive interference effects for logic inversion for a passive configuration without the use of electro-optic or thermo-optic tuning.
- Electromagnetic simulations confirm transmission inversion, from which 2-input NAND and NOR gates are approximated. SEM imaging confirms CMOS fabrication compatibility thanks to intentional design.

Custom 3D Printed Nerf Blaster "Warthog" | *Baja Blasters (Personal)* Dec 2025 – Aug 2026

- Designed a 4-layer printed circuit board in KiCad, incorporating an RP2040 to drive an electronic speed controller for two brushless motors, with a fast decay circuit for a solenoid pusher for fire rates up to 25 darts per second.
- Wrote purpose-built firmware (C++) for general operation, motor PID tuning, reconfigurable user profile settings, memory management, and an I2C OLED screen for user interaction and system feedback.

RISC-V 32I Processor | *Florida Polytechnic University* Mar 2025 – May 2025

- Constructed a single-core RV32I processor in the Intel Quartus Prime FPGA SDK, implementing 10 arithmetic and branch logic instructions.
- Validated on DE-10 Lite FPGA board through purpose written assembly program to recursively calculate the Fibonacci sequence for 16 iterations.

LEADERSHIP EXPERIENCE & AWARDS

Leadership: Phoenix Autonomy Electrical Lead (Jan 2026 – Present), Phoenix Autonomy Battery Lead (Aug 2025 – Dec 2026), Poly Concert Band Vice Captain (Aug 2024 – Present), Violet Voices Choir Bass Section Lead (Aug 2024 – May 2025), Presidential Ambassador (Jan 2023 – May 2025).

Awards: 1st Place Research Presentation – Second Annual Poly Research Day, 1st Place Paper Presentation – Second Annual Student Research Symposium IEEE Student Branch, IEEE-HKN Honor Society Member, President's & Provost's List, Saddle Creek Logistics Scholar, Florida Bright Futures Academic Scholar.

SKILLS

Languages: C, C#, C++, Python, Embedded C, MIPS assembly, Verilog & SystemVerilog, JavaScript.

Software: Klayout, Electric, Tidy3D, MATLAB, KiCad, STM32CubeIDE, Microchip Studio, Intel Quartus Prime, Multisim, LTspice, Visual Studio, SolidWorks (CSWA).

Hardware: GDSII Layout, PCB Layout, FPGA programming, microcontroller embedded programming, real-time operating systems (RTOS), oscilloscope & function generator proficiency, soldering, 3D modeling & printing.

Relevant Coursework: Optoelectronics, VLSI Design, Embedded Operating Systems, Computer Architecture and Organization, Microprocessors, Object Oriented Programming, Data Structures and Algorithms, Digital Logic Design, Digital Electronics, Electronic Motor Control.